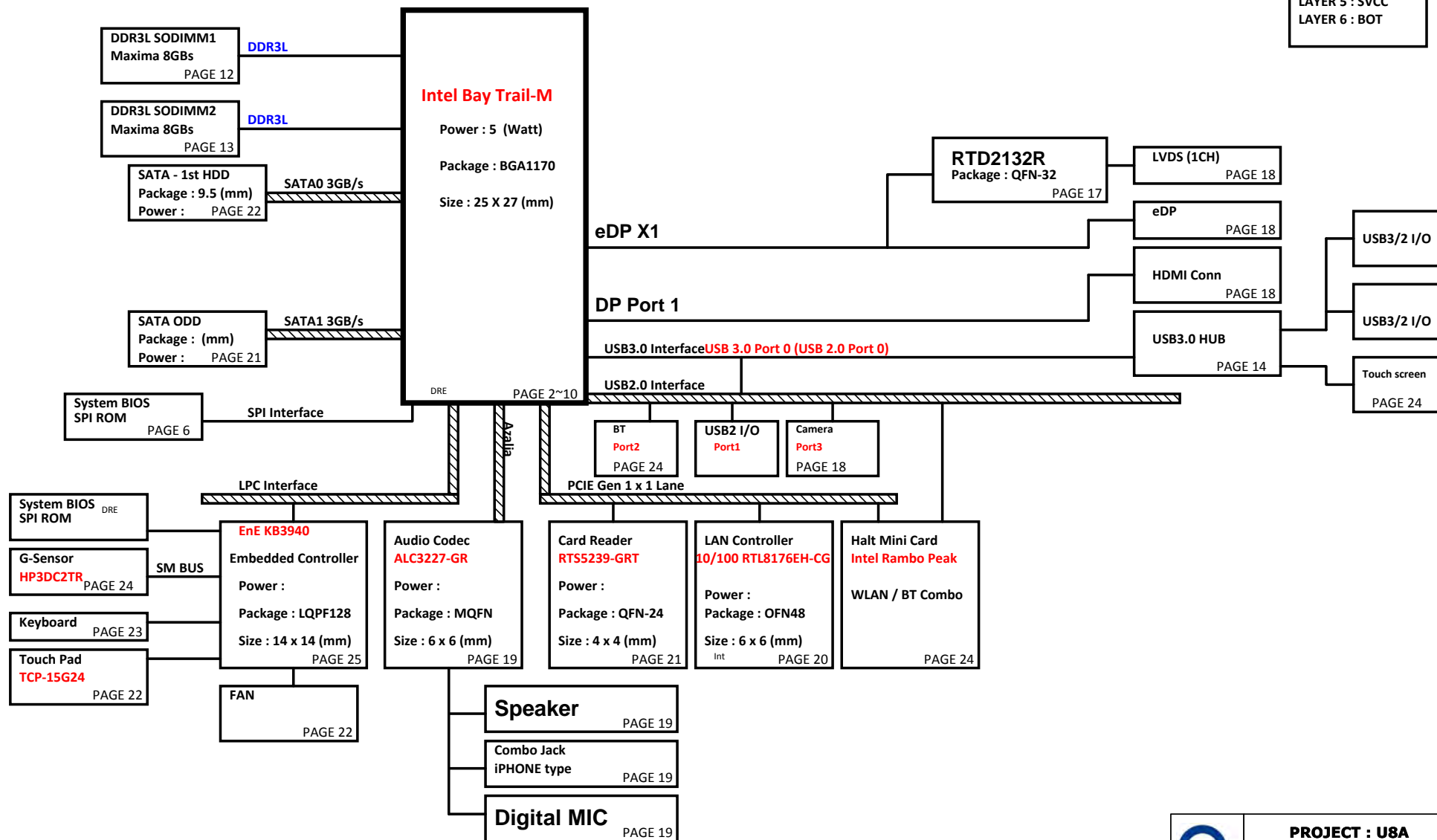


U87/U88 UMA (14"/15.6") Ultra/Slim Intel Bay trail-M Platform Block Diagram

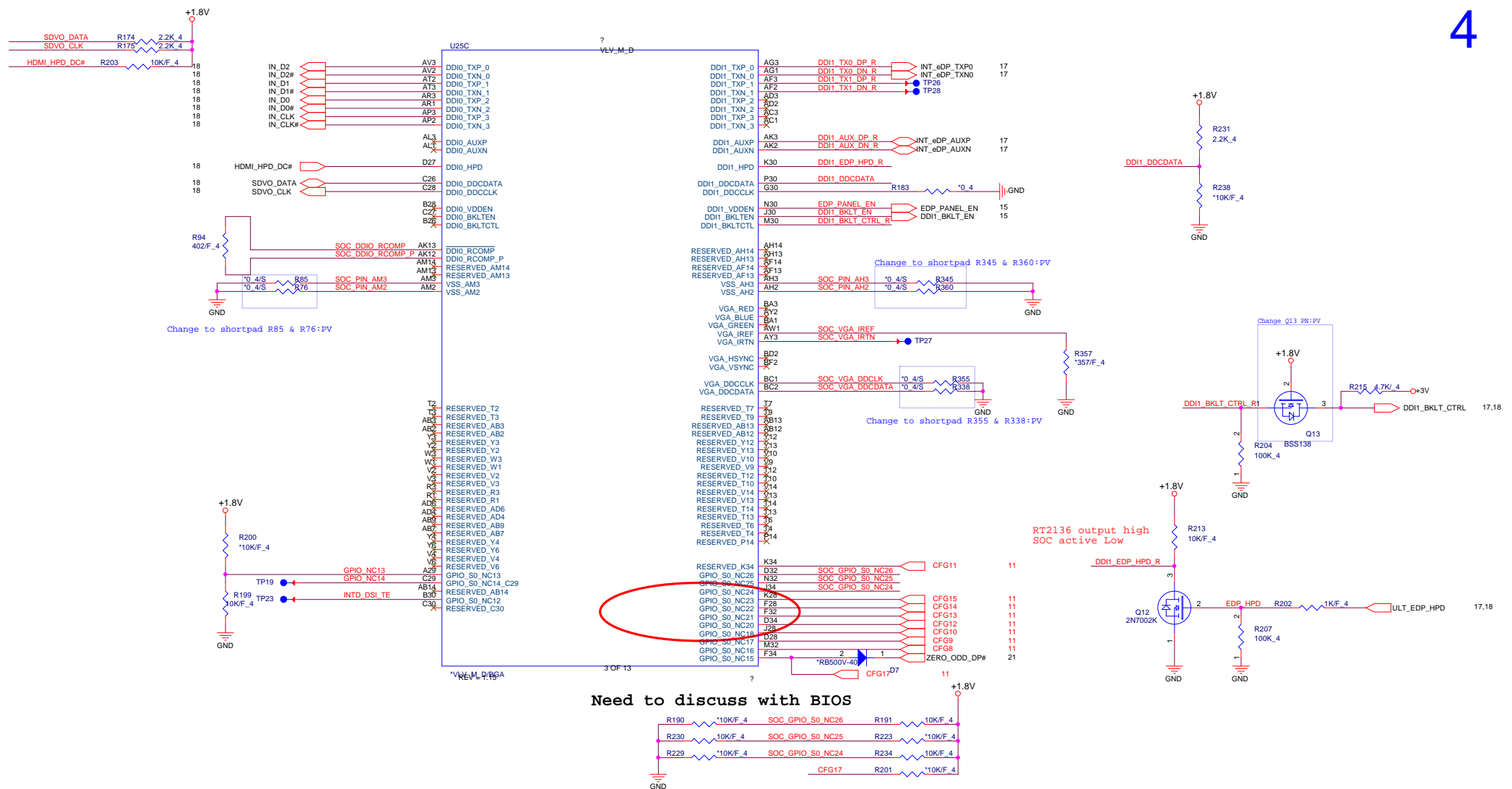
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

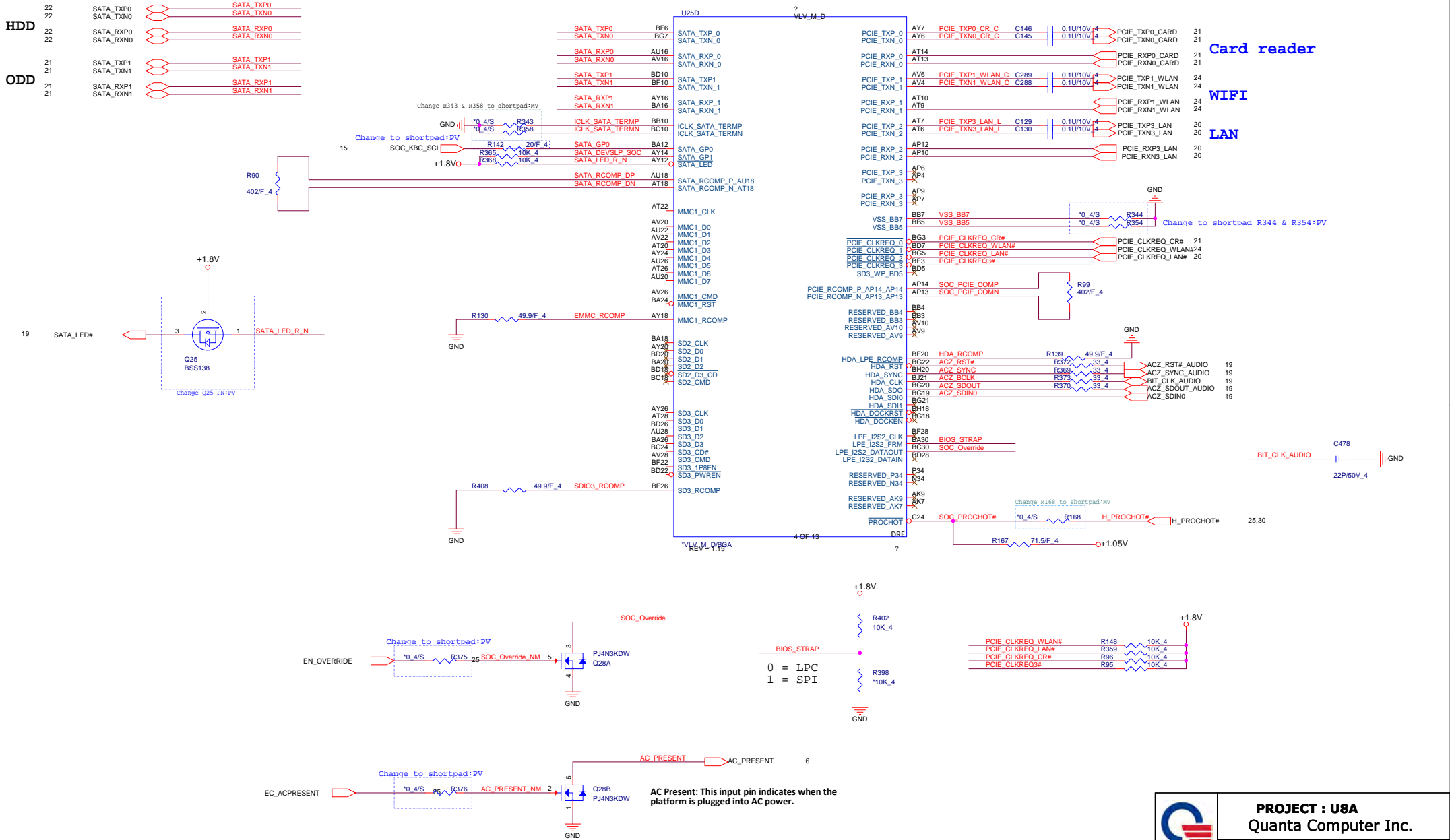






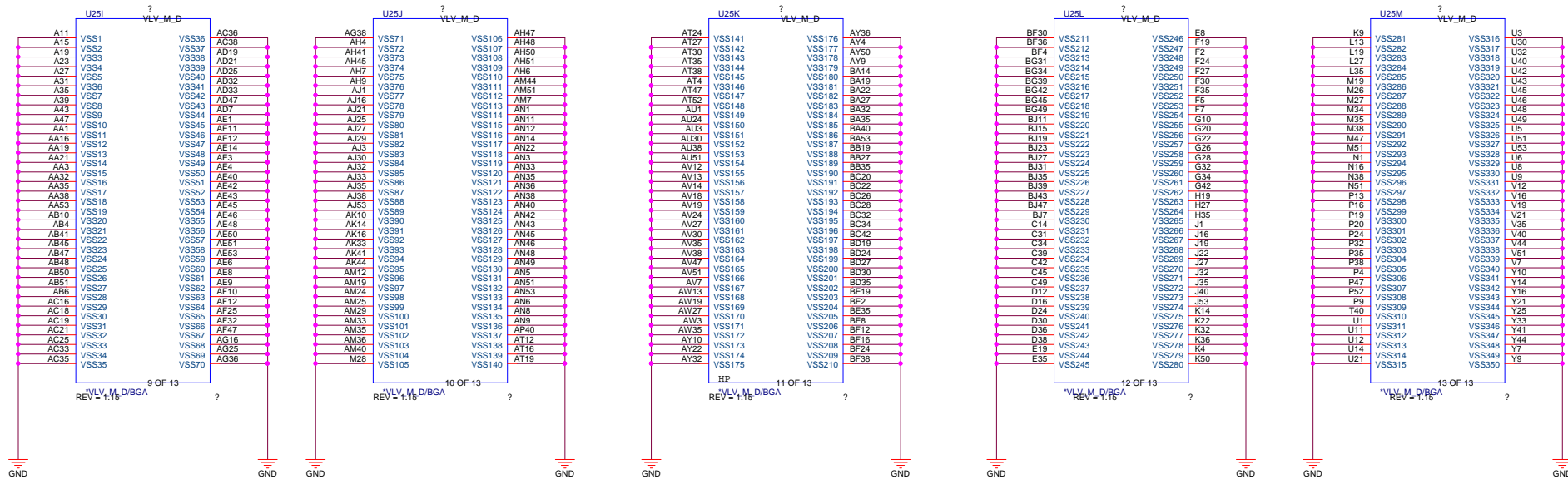


GPIO26	0	1	0=W/FAN , 1=Fanless
GPIO25	0	0	
GPIO24	0	1	0=14", 1=15"



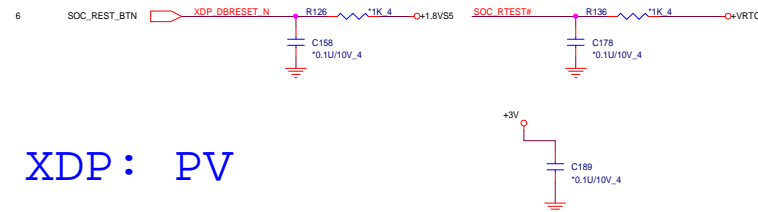
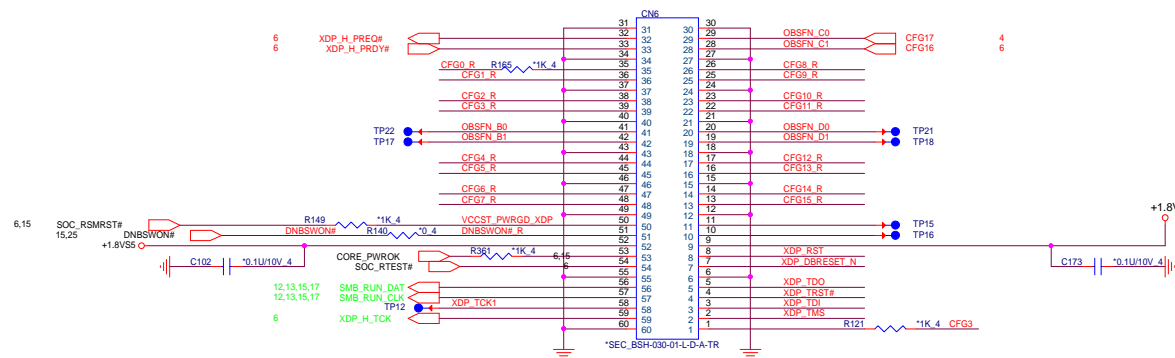




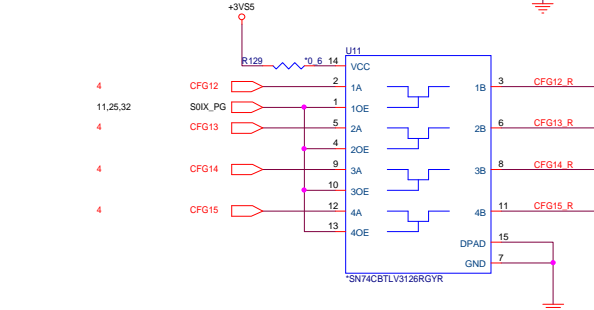
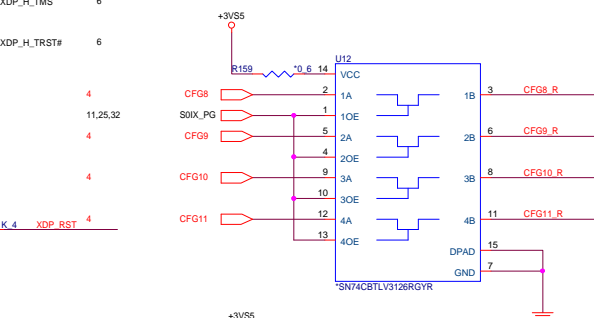
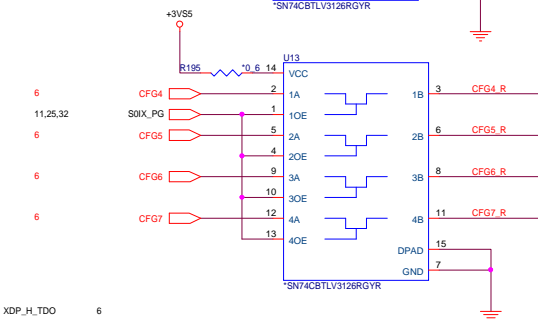
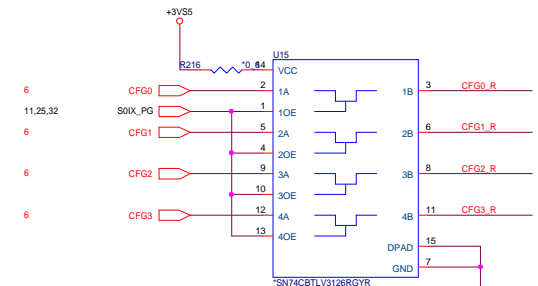
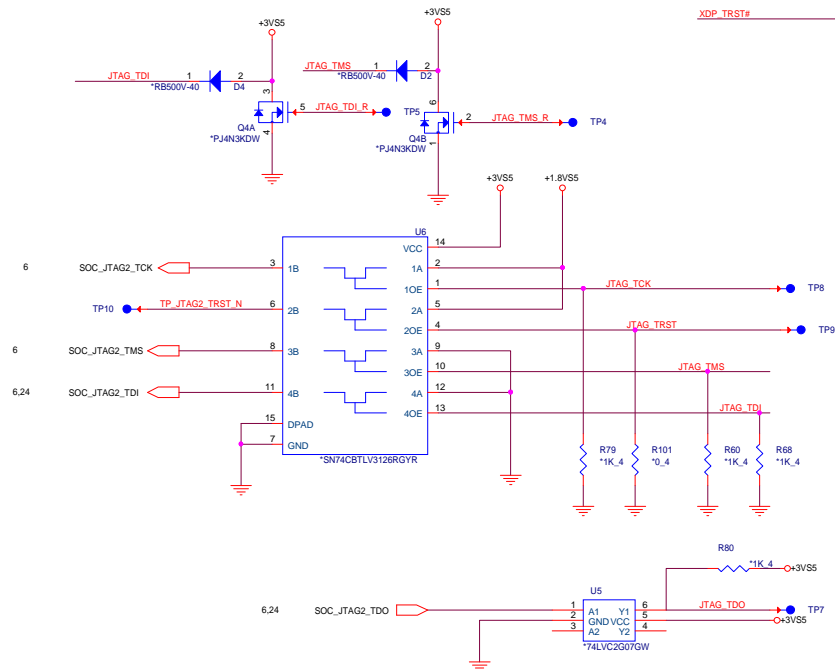


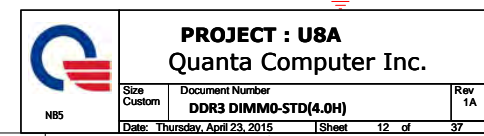
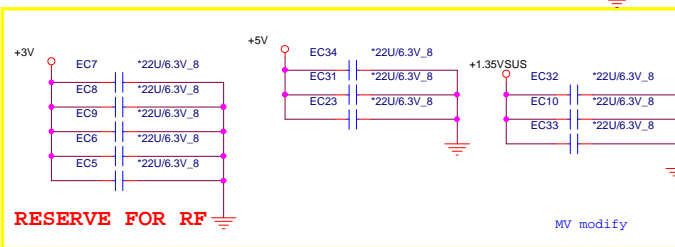
PROJECT : U8A
Quanta Computer Inc.

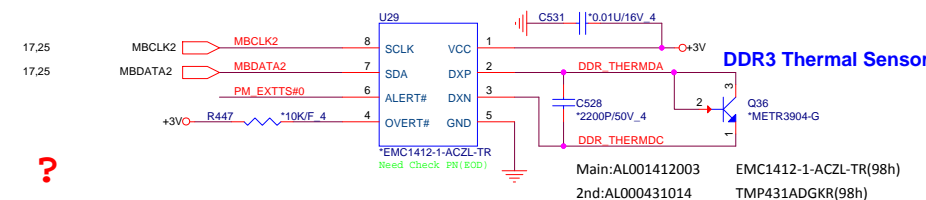
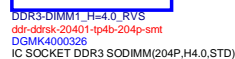
Size	Document Number	Rev
Custom	Valley 9/9 (GND)	1A
Date: Thursday, April 23, 2015	Sheet 10 of 37	



Un-stuff XDP: PV







VREF DQ1 M1 Solution

12.29

DDR_VTTREF

+1.35V_SUS

R260

*0.6

R264

4.7K/_4

SMDDR_VREF DO1_M1

R263

4.7K/_4

C302

0.1U/10V_4

+1.35V_SUS

R274

*0.6

R270

4.7K/_4

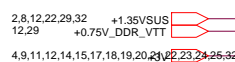
R269

+SMDR_VREF DIMM2

C334

0.1U/10V_4

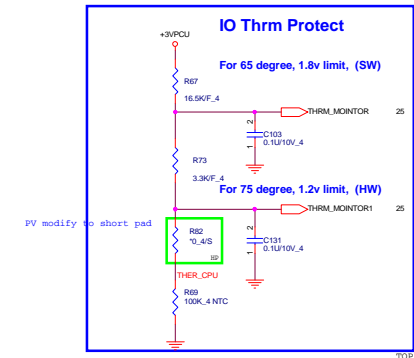
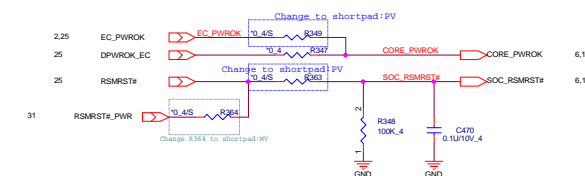
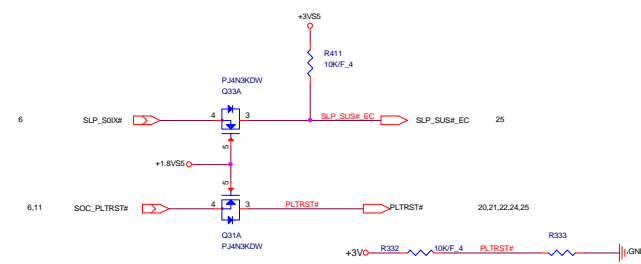
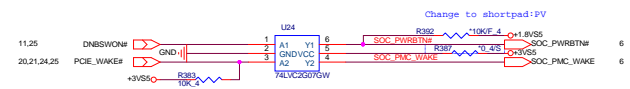
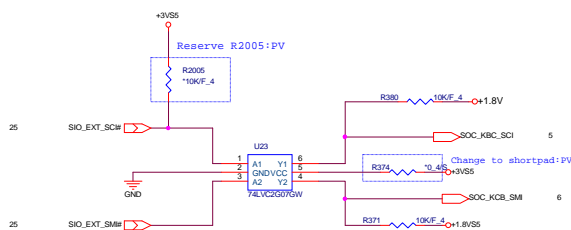
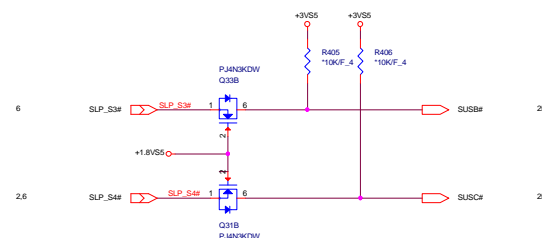
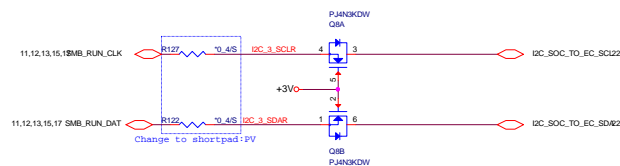
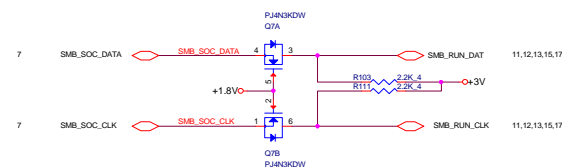
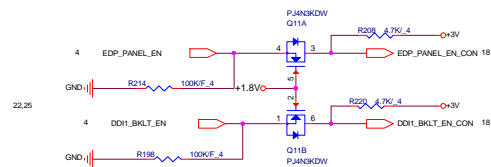
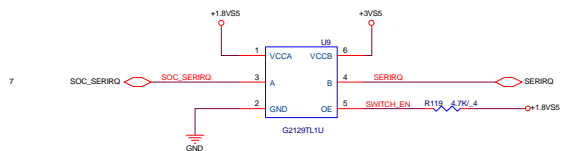
Change R264, R263, R270, R269 to 4.7K ohm:PV



PROJECT : U8A
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM1-STD(4.0H)	Rev 1A
Date: Thursday, April 23, 2015	Sheet 13 of 37	





S5 to S0 Cold Boot Sequence without S0ix

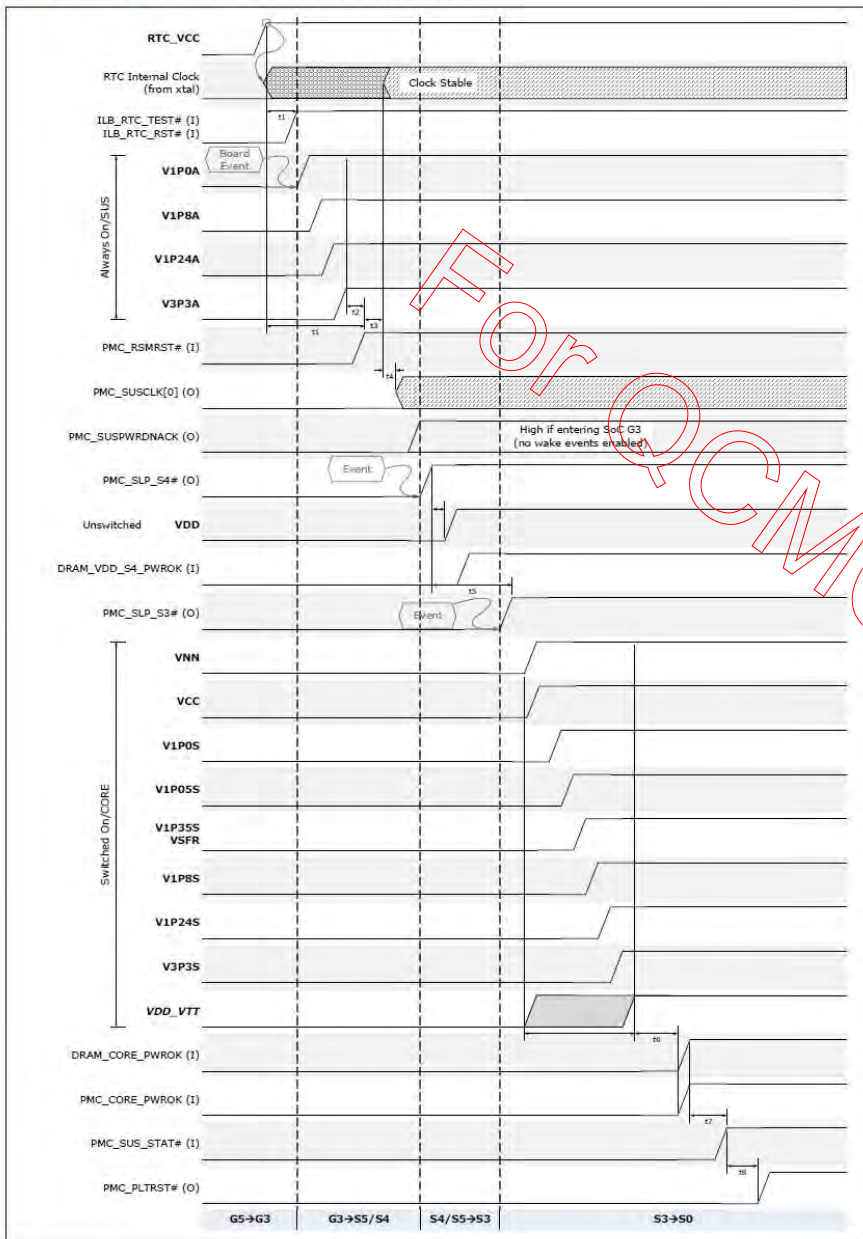
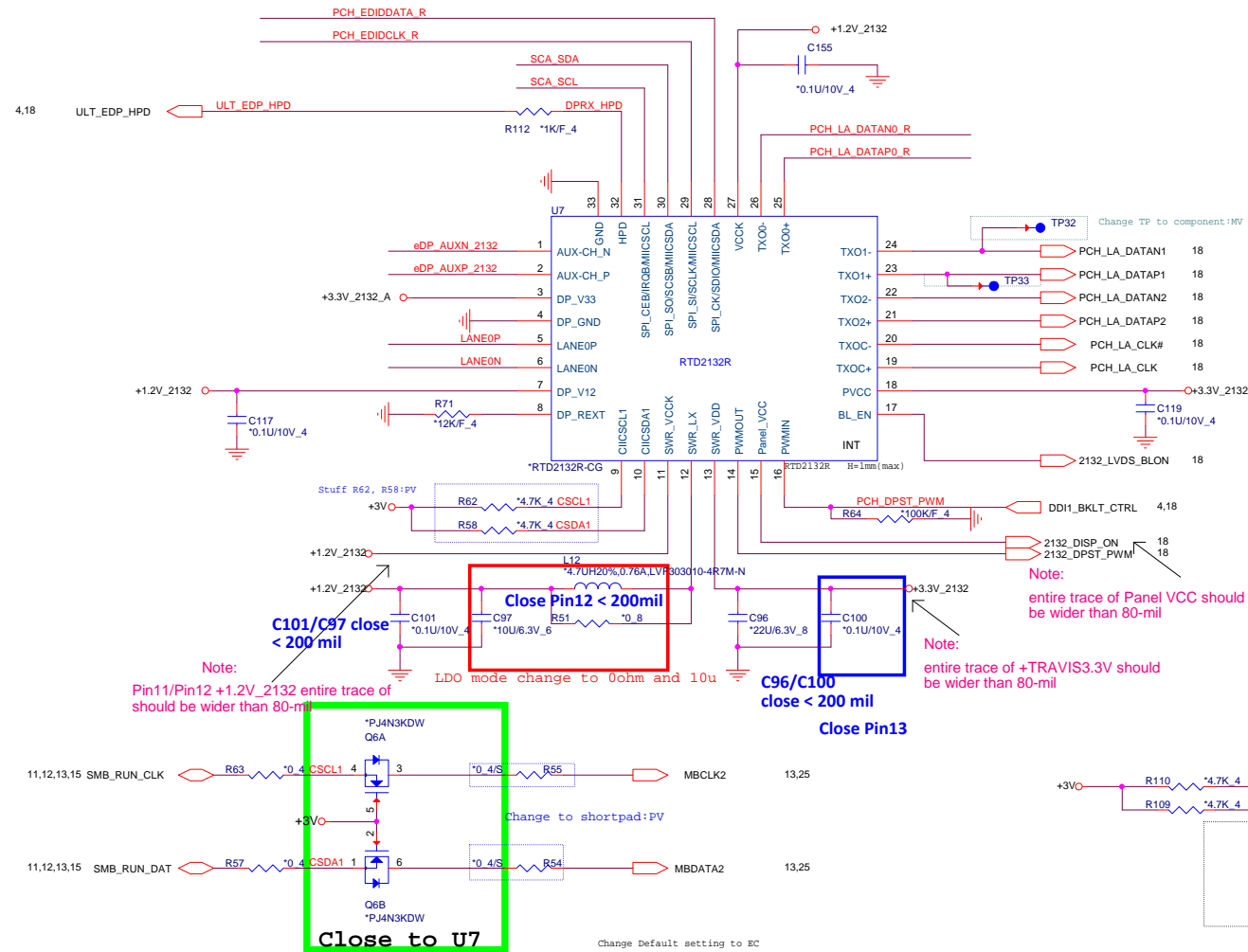
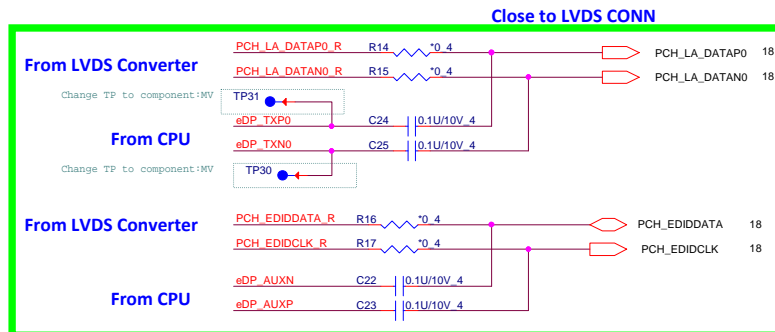
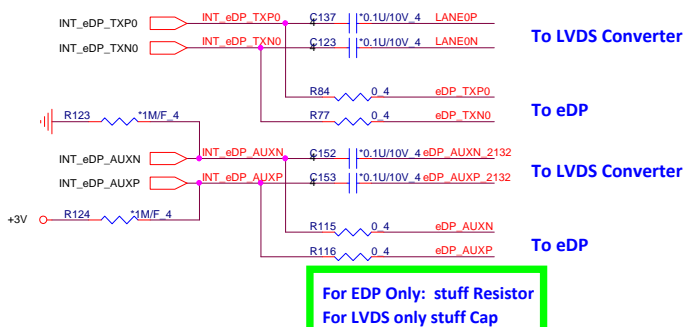


Table 4-12. Cold Boot Timing Spec

Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us
T3	VSUS stable to PMC_RSMRST# high	10			ms
T4	S and SX rails stable to PMC_CORE_PWROK	100			ms

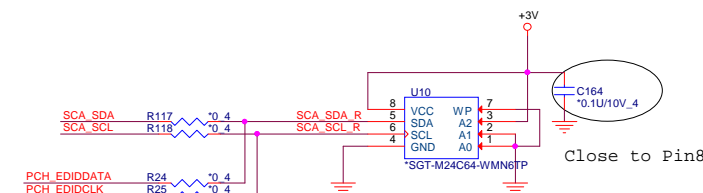
NOTES:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
2. Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
3. Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.



SCA_SCL pull high => EEPROM mode
SCA_SDA pull low => EEPROM Free mode

Address=0xA8

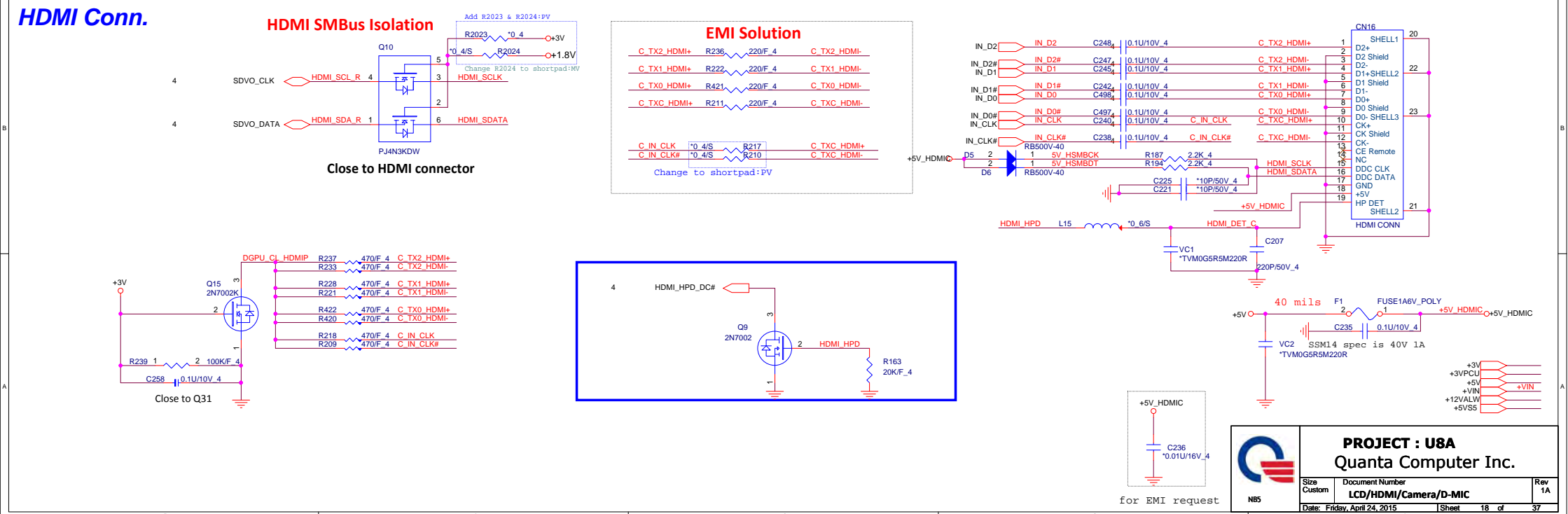
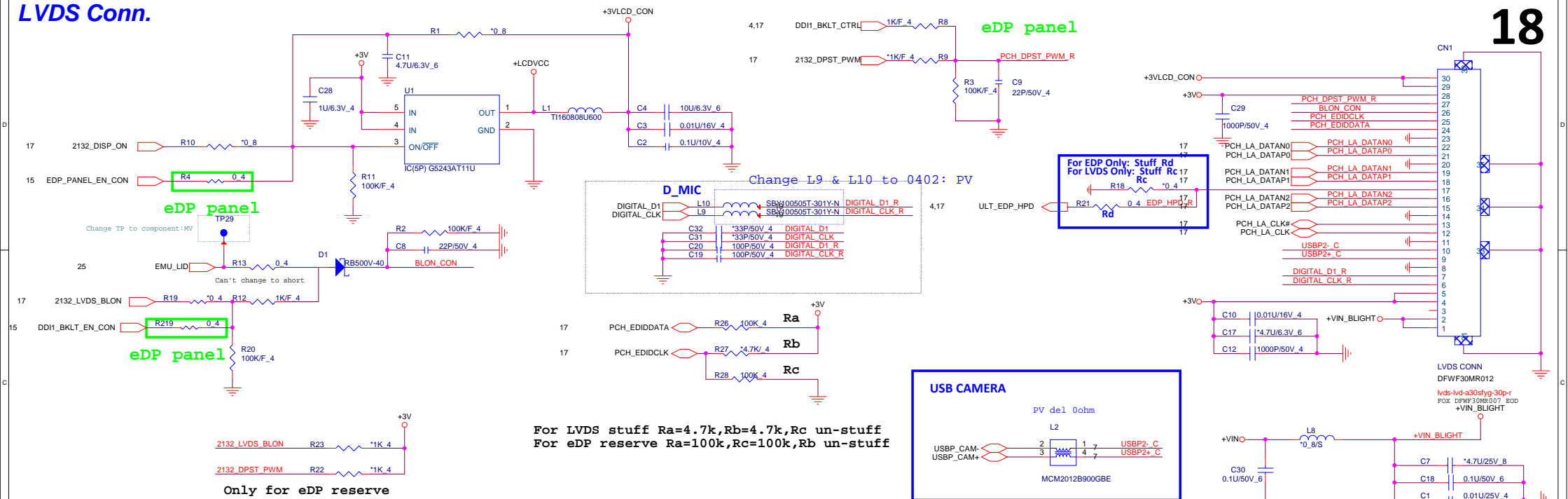


RTD2132S => R117, R118
RTD2132R => R24, R25

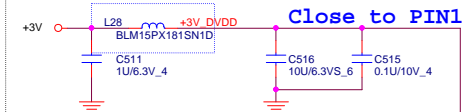
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

PROJECT : U8A Quanta Computer Inc.		
Size	Document Number	Rev
Custom	LVDS converter RTD2132R	1A
Date: Thursday, April 23, 2015	Sheet 17 of 37	

EE PROM U10
EC OPTION Q6, R55, R54

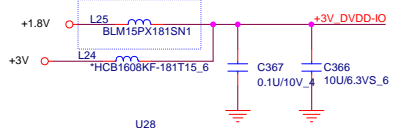


Change L29 to 0402: PV



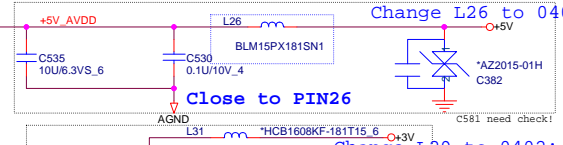
Close to PIN1

Change L25 to 0402: PV



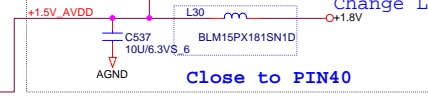
>40mils trace

Change L26 to 0402: PV



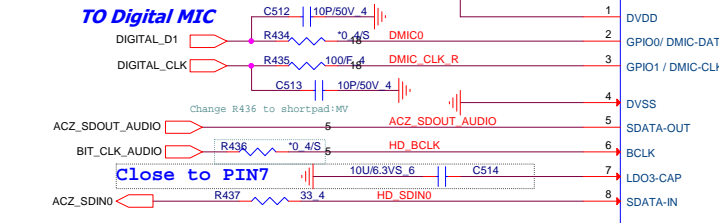
Close to PIN26

Change L29 to 0402: PV

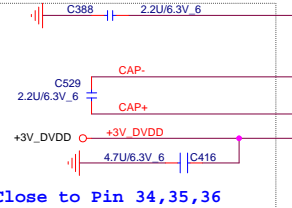
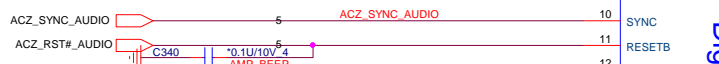


Close to PIN40

TO Digital MIC

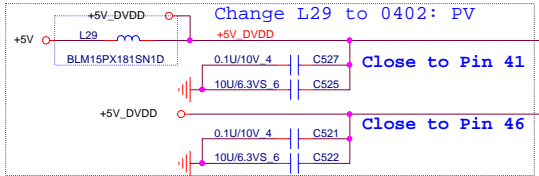


Close to PIN7



Close to Pin 34,35,36

TO Internal Speakers

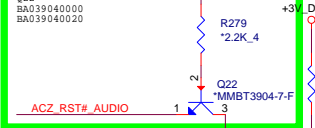


Change L29 to 0402: PV

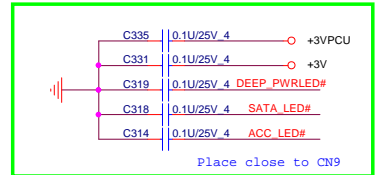
Close to Pin 41

Close to Pin 46

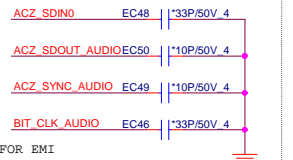
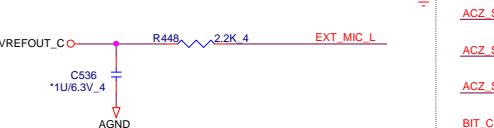
for intel HSW ULT



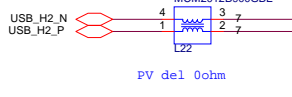
USB 2.0 AND AUDIO COMBO JACK



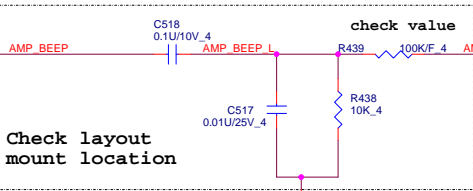
Place close to CN9



FOR EMI

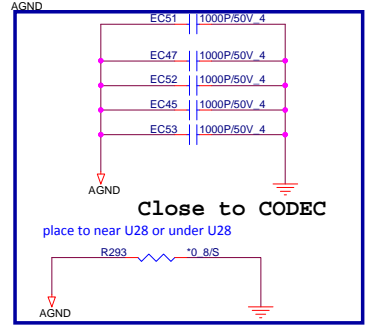
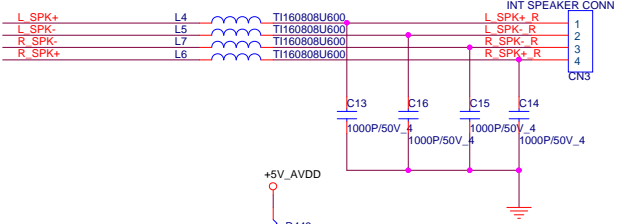


PV del 0ohm



Check layout mount location

Close to Speaker
Speaker 4 ohm: 40mils



Close to CODEC

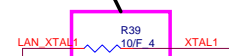
place to near U28 or under U28



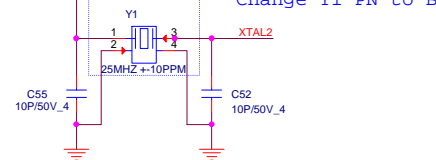
PROJECT : U8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalla ALC 3227	1A
Date: Thursday, April 23, 2015	Sheet 19 of 37	

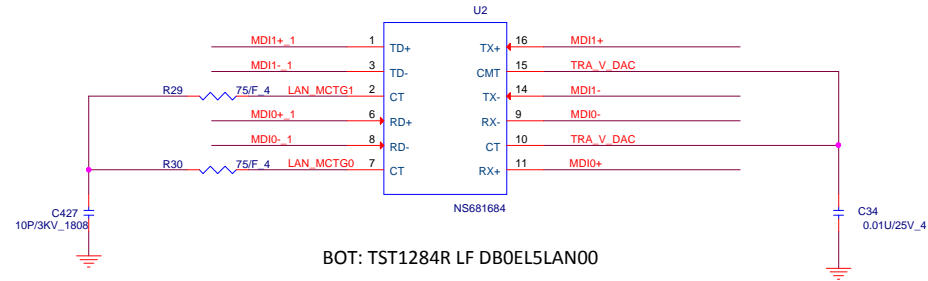
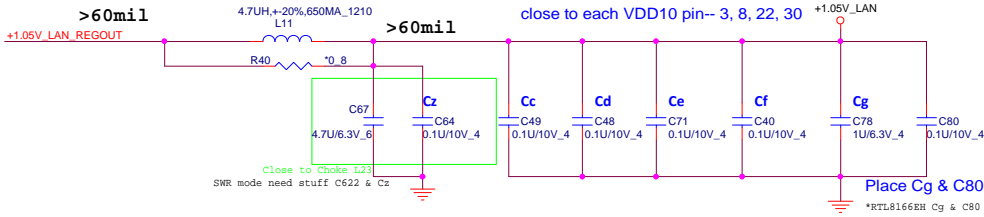
For EMI 0 ~ 22 ohm



Change Y1 PN to BG625000121: PV

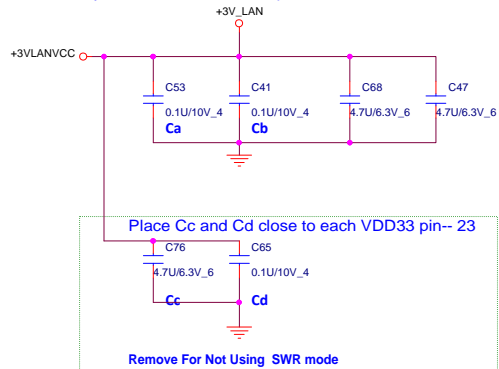


Trace < 30 mil
Width > 60 mil
Power trace Layout 宽度 > 60mil



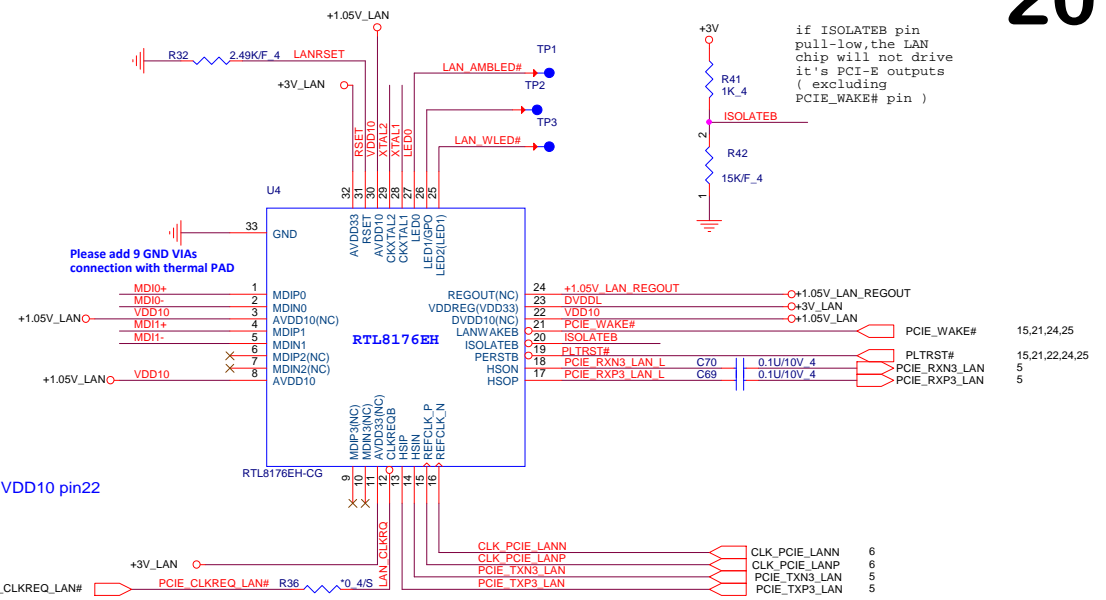
BOT: TST1284R LF DB0EL5LAN00

Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

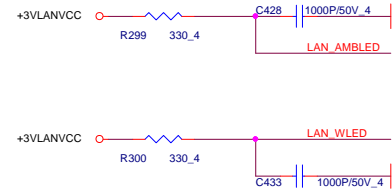
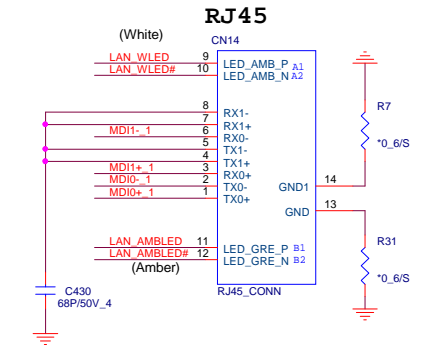


4,9,11,12,13,14,15,18,19,21,22,23,24,25,32

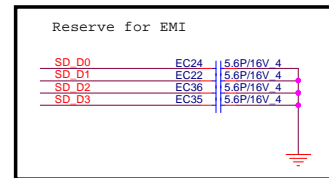
+3VLANVCC



LAN conn

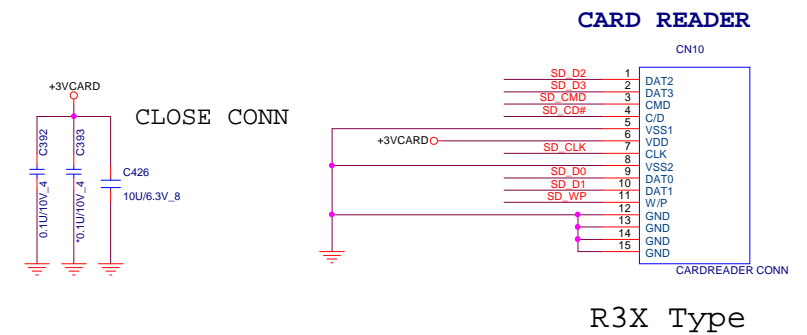


NB5	PROJECT : U8A Quanta Computer Inc.		
	Size Custom	Document Number LAN RTL8176EH/RJ45	Rev 1A
	Date: Thursday, April 23, 2015	Sheet 20 of	37

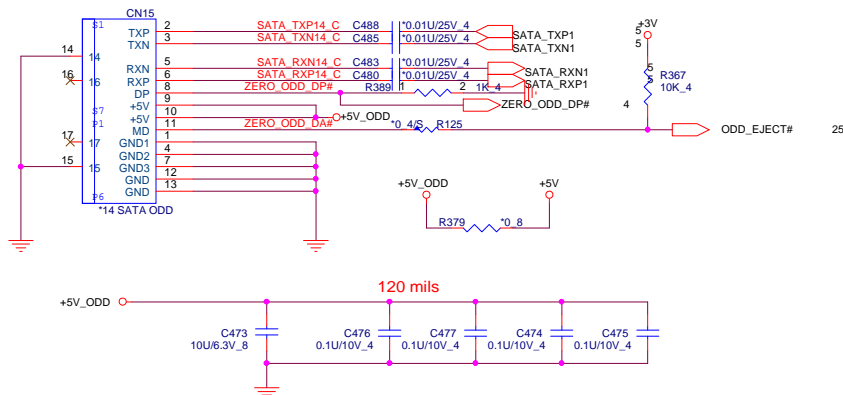


SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

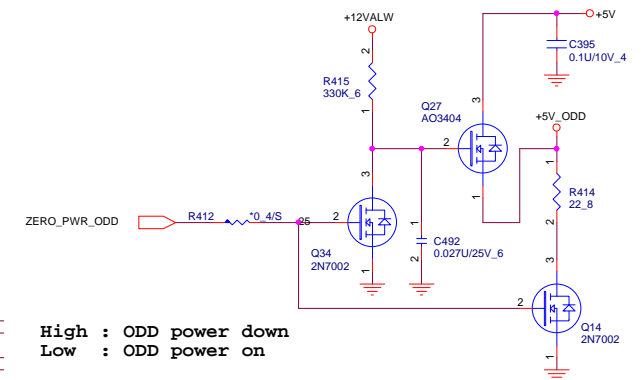
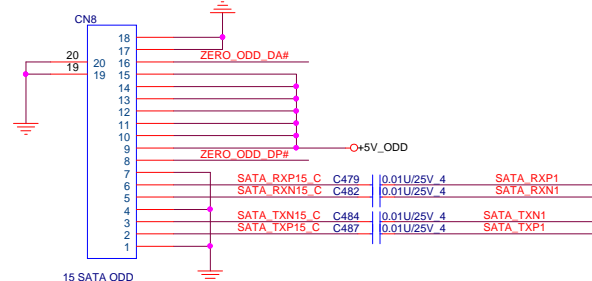
SD / MMC



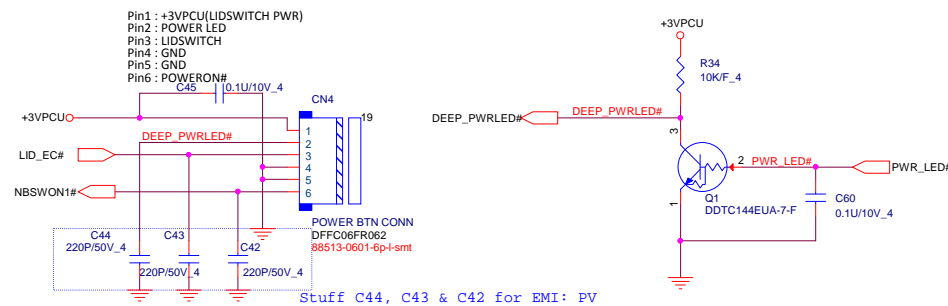
Bypass CAP close conn



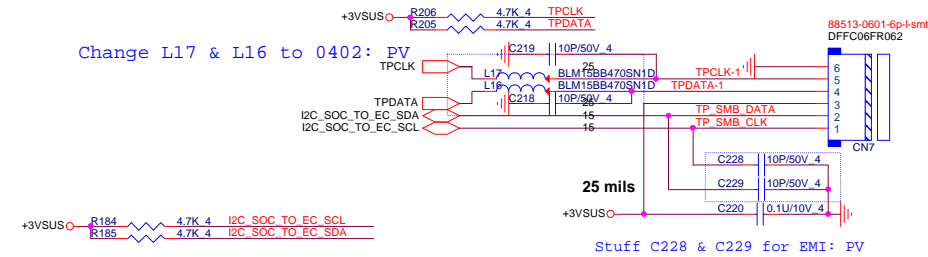
New Type



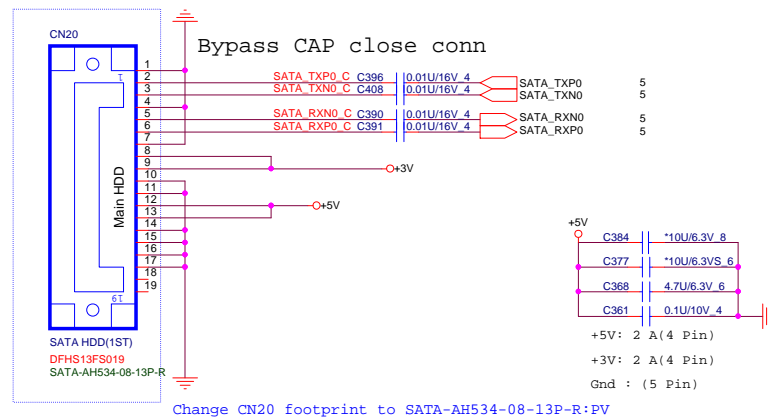
Power Button Connector



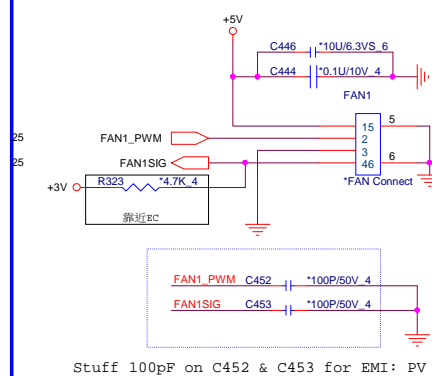
Touch Pad Connector



SATA HDD Connector(Cable type)

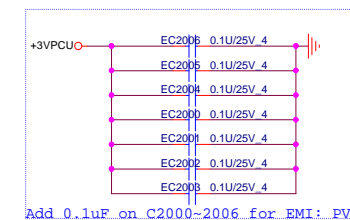


FAN



Mini PCI-E Card 2- Full size mSATA

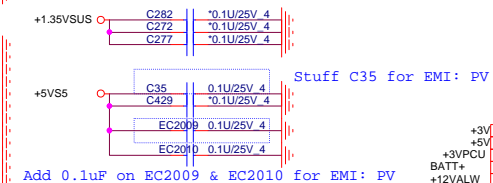
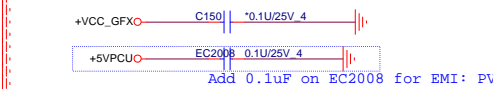
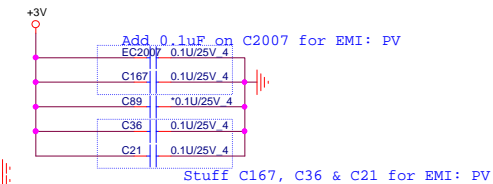
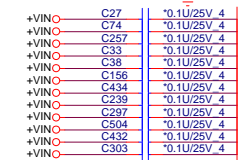
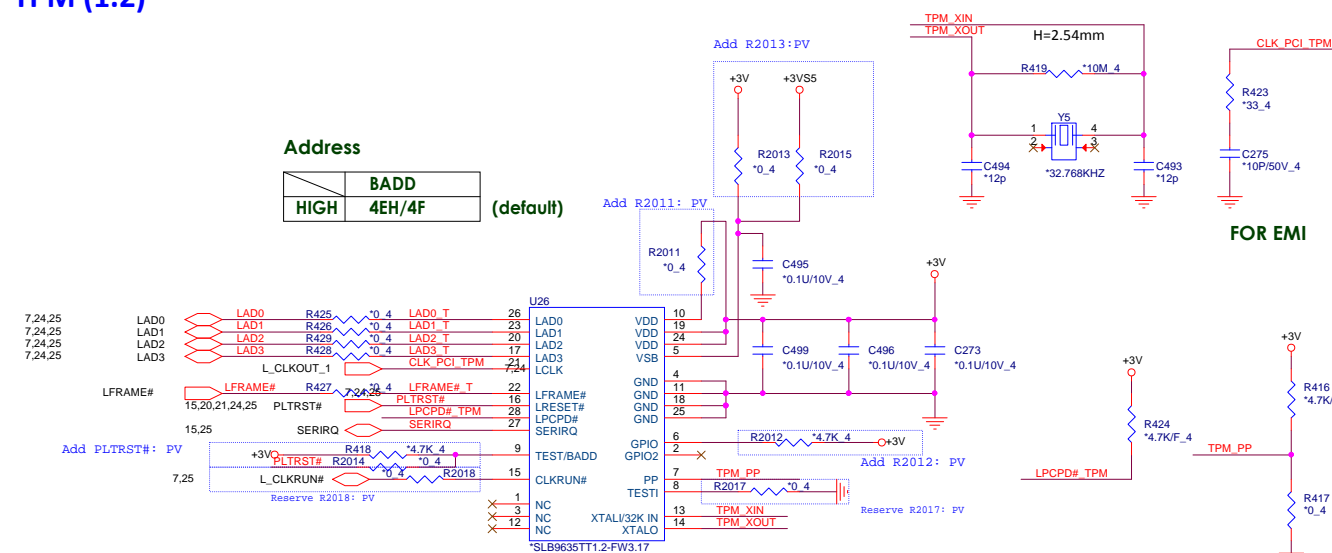
Removed mSATA 6/19



TPM (1.2)

Address

	BADD
HIGH	4EH/4F (default)



		PROJECT : U8A	
		Quanta Computer Inc.	
Size Custom	Document Number	HDD/mSATA/FAN/LED	
Date: Thursday, April 23, 2015	Sheet	22 of	37

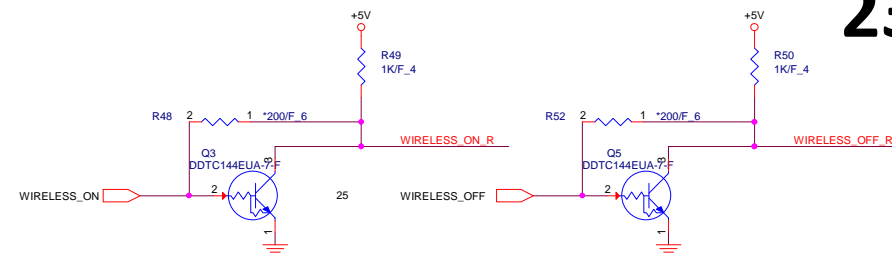
[illegible]

The diagram illustrates the keyboard pull-up circuit. It features two 8-pin connectors, RP2 and RP1, each with a 10kΩ pull-up resistor connected to a +3VPCU supply. The pins are connected to various MY pins as follows:

- RP2:**
 - Pin 1: MY14
 - Pin 2: MY11
 - Pin 3: MY10
 - Pin 4: MY15
 - Pin 5: (unlabeled)
 - Pin 6: MY6
 - Pin 7: MY3
 - Pin 8: MY2
 - Pin 9: MY13
- RP1:**
 - Pin 1: MY2
 - Pin 2: MY4
 - Pin 3: MY7
 - Pin 4: MY8
 - Pin 5: (unlabeled)
 - Pin 6: MY9
 - Pin 7: MY0
 - Pin 8: MY5
 - Pin 9: MY1

At the bottom, there are two additional pull-up resistors:

- R313: 8.2K 4MY16
- R309: 8.2K 4MY17



The schematic illustrates the internal clamp diode network for various USB pins. Each pin is connected to a series of three diodes (labeled Cxxx) that lead to ground. The diodes are oriented such that they can clamp both positive and negative voltage transients. The labels for each set of diodes are as follows:

- C308**: Labeled "USB30_TX1- C C308" and "*Clamp-Diode".
- C299**: Labeled "USB30_TX1+ C C299" and "*Clamp-Diode".
- C309**: Labeled "USBP0- C C309" and "*Clamp-Diode".
- C312**: Labeled "USBP0+ C C312" and "*Clamp-Diode".
- C320**: Labeled "USB30_RX1- C C320" and "*Clamp-Diode".
- C315**: Labeled "USB30_RX1+ C C315" and "*Clamp-Diode".
- C278**: Labeled "USBP5- C C278" and "*Clamp-Diode".
- C283**: Labeled "USBP5+ C C283" and "*Clamp-Diode".
- C286**: Labeled "USB3.0 HUB_RX C286" and "*Clamp-Diode".
- C285**: Labeled "USB3.0 HUB_RX C285" and "*Clamp-Diode".

In addition, there are two unlabeled sets of diodes connected to "USB3.0_HUB_TX_C227B" and "USB3.0_HUB_TX_C227R".

[illegible]

USB 3.0

C506 0.1U/10V .4
C507 470P/50V .4
VC4 1AV/LCSS .4
C500 1000P/50V .4

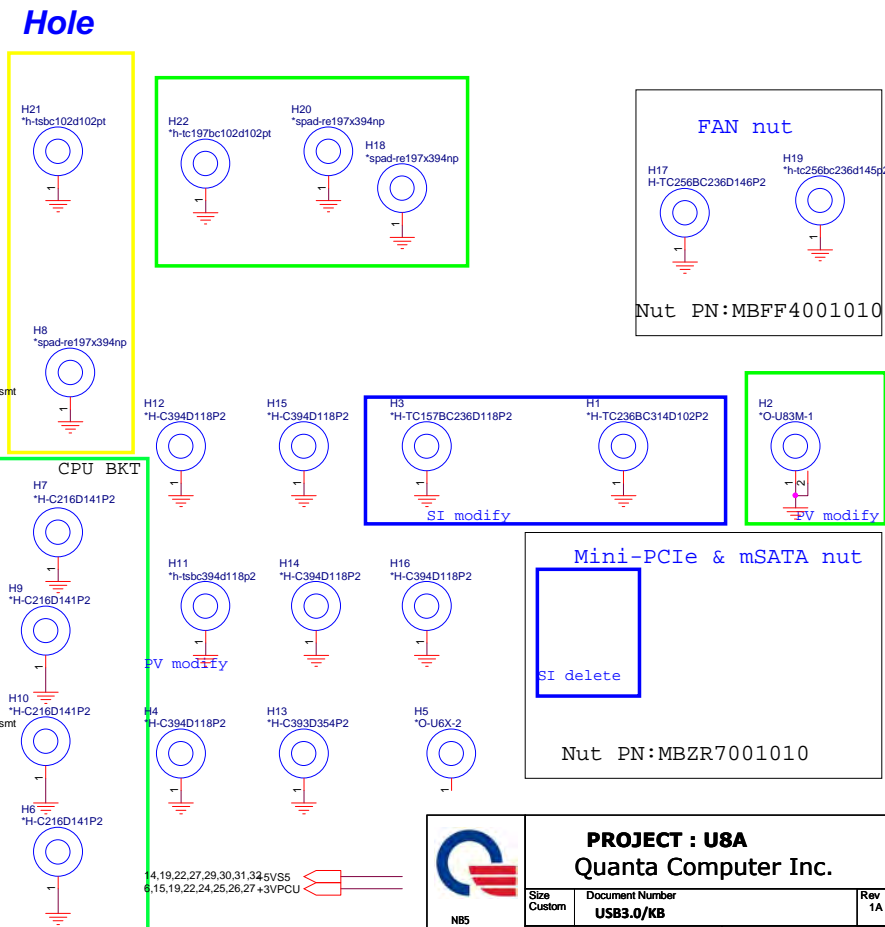
+5V USBP0-
USBP0+ C
USB30 RX1- C
USB30 RX1+ C
USB30 TX1- C
USB30 TX1+ C

1A

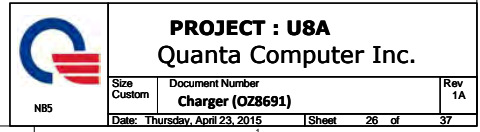
CN19 USB3.0 CONN

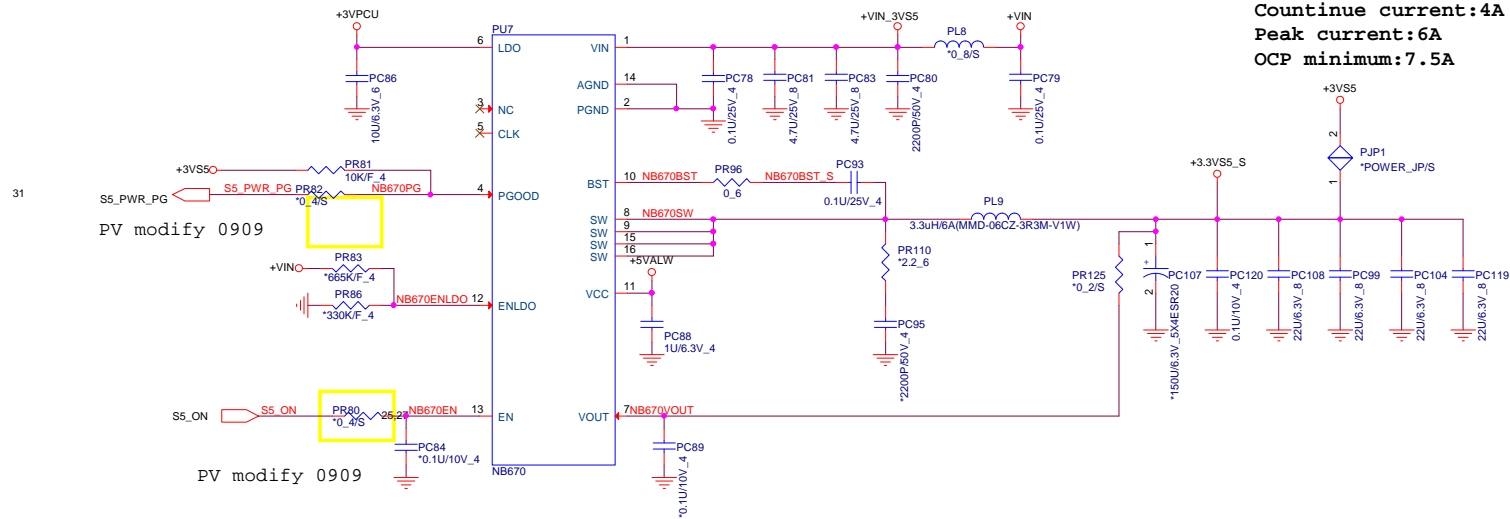
1 1VBUS
2 D-
3 D+
4 GND
5 SSRX+
6 SSRX-
7 GND
8 SSTX-
9 SSTX+
10
11
12
13

DFH0509R435
20120202002014

[illegible]

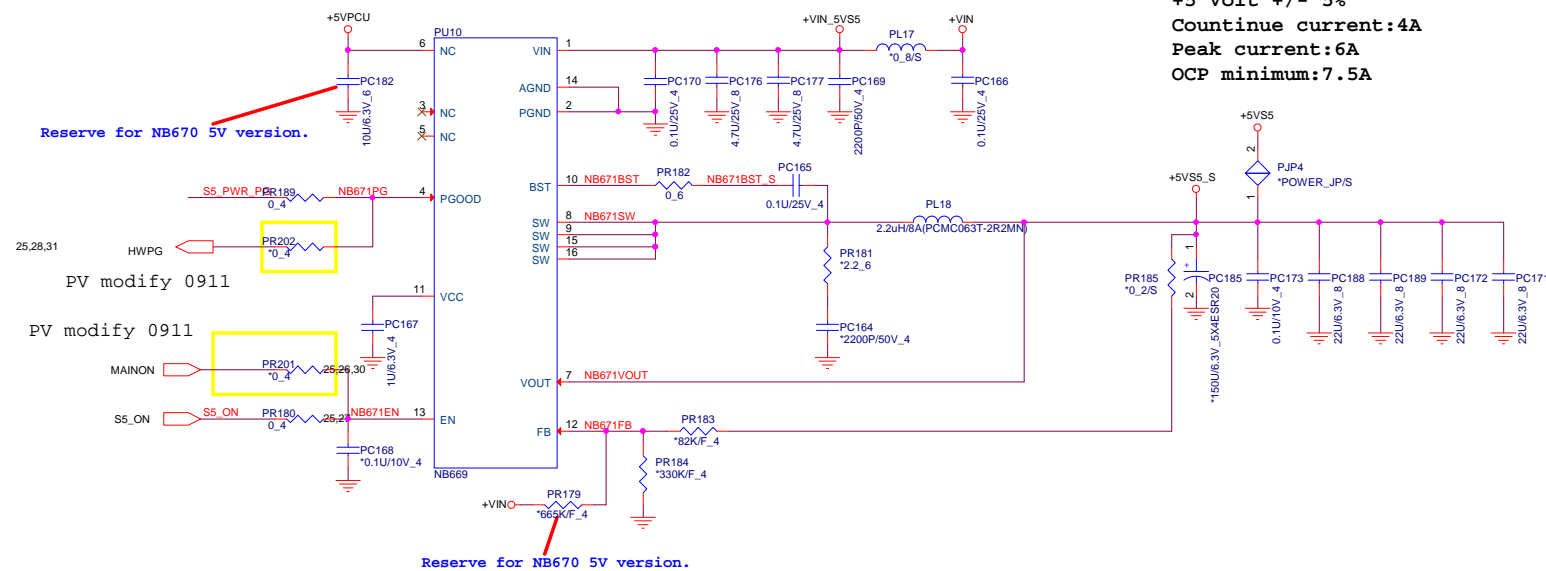






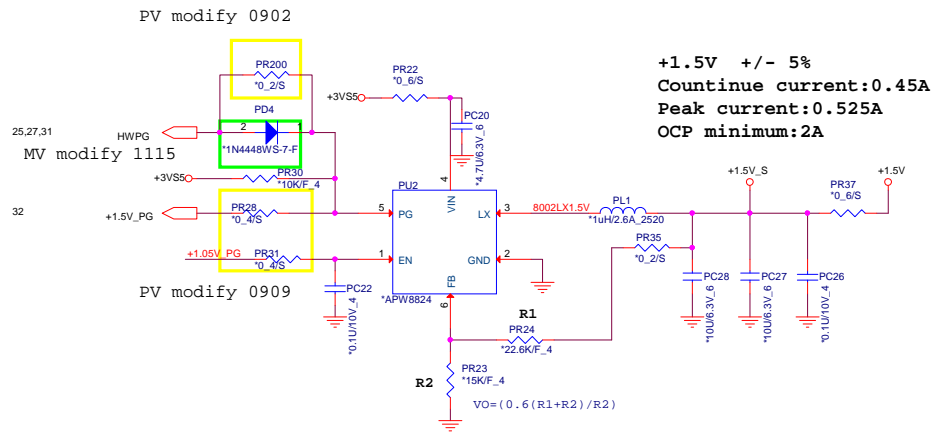
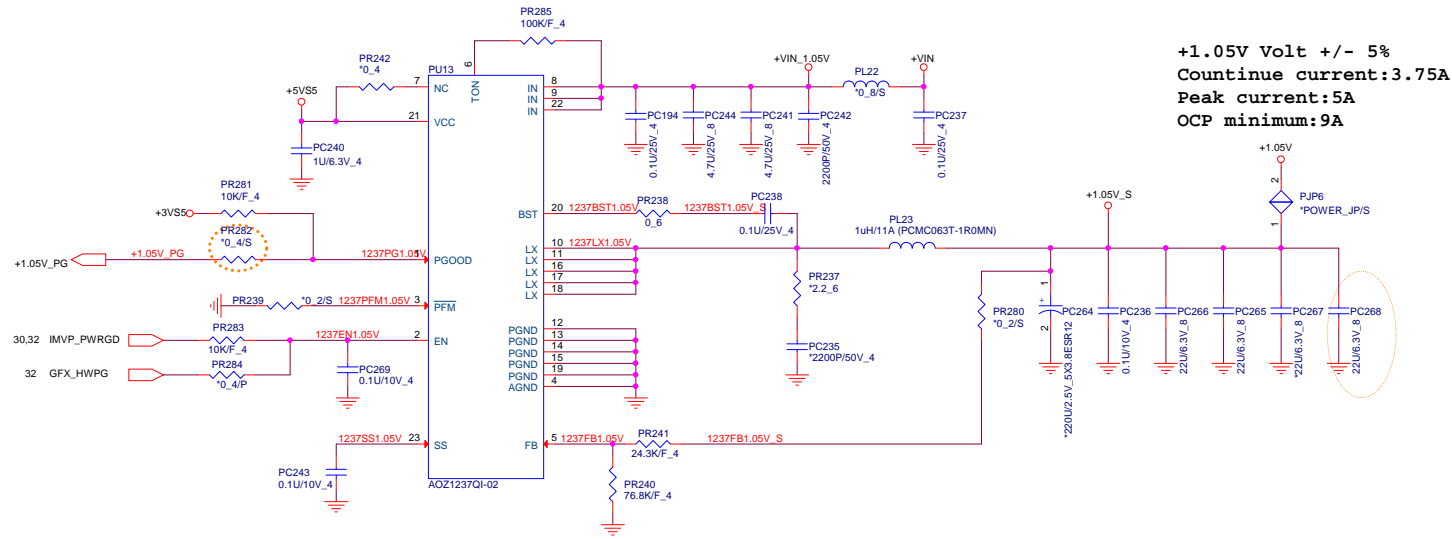
+3VS5
+5VS5

2,9,11,14,15,22,24,28,30,31,32
14,19,22,23,29,30,31,32



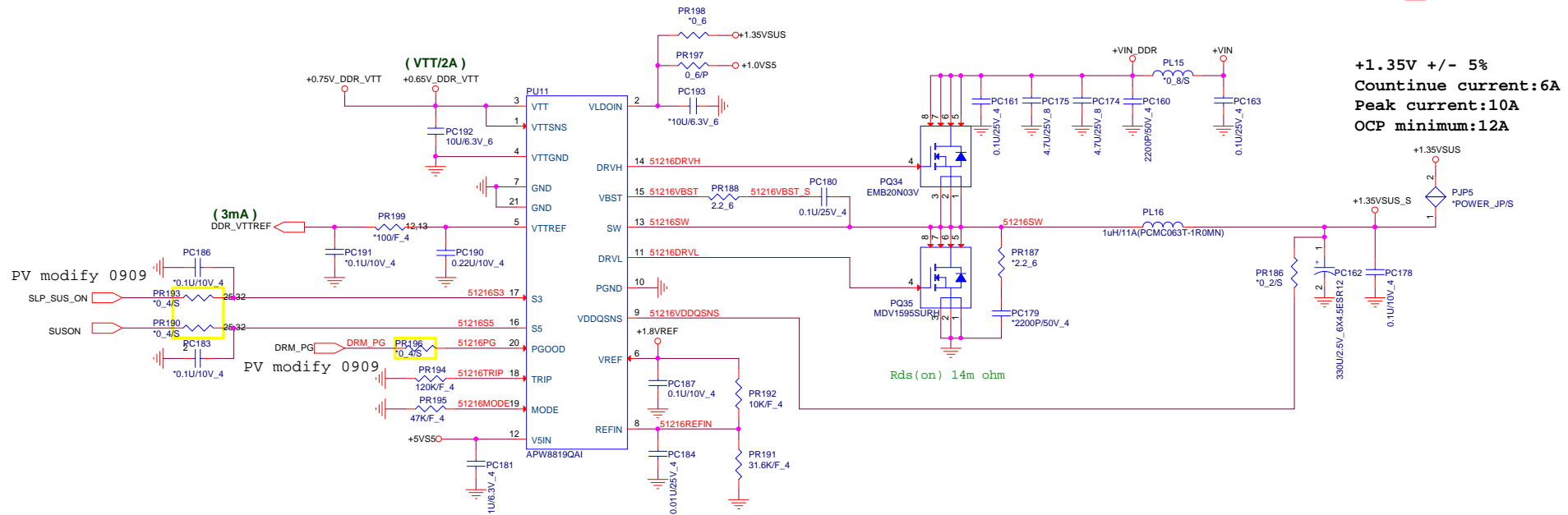
PROJECT : U8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(NB670/NB669)	1A
Date: Thursday, April 23, 2015	Sheet 27 of 37	

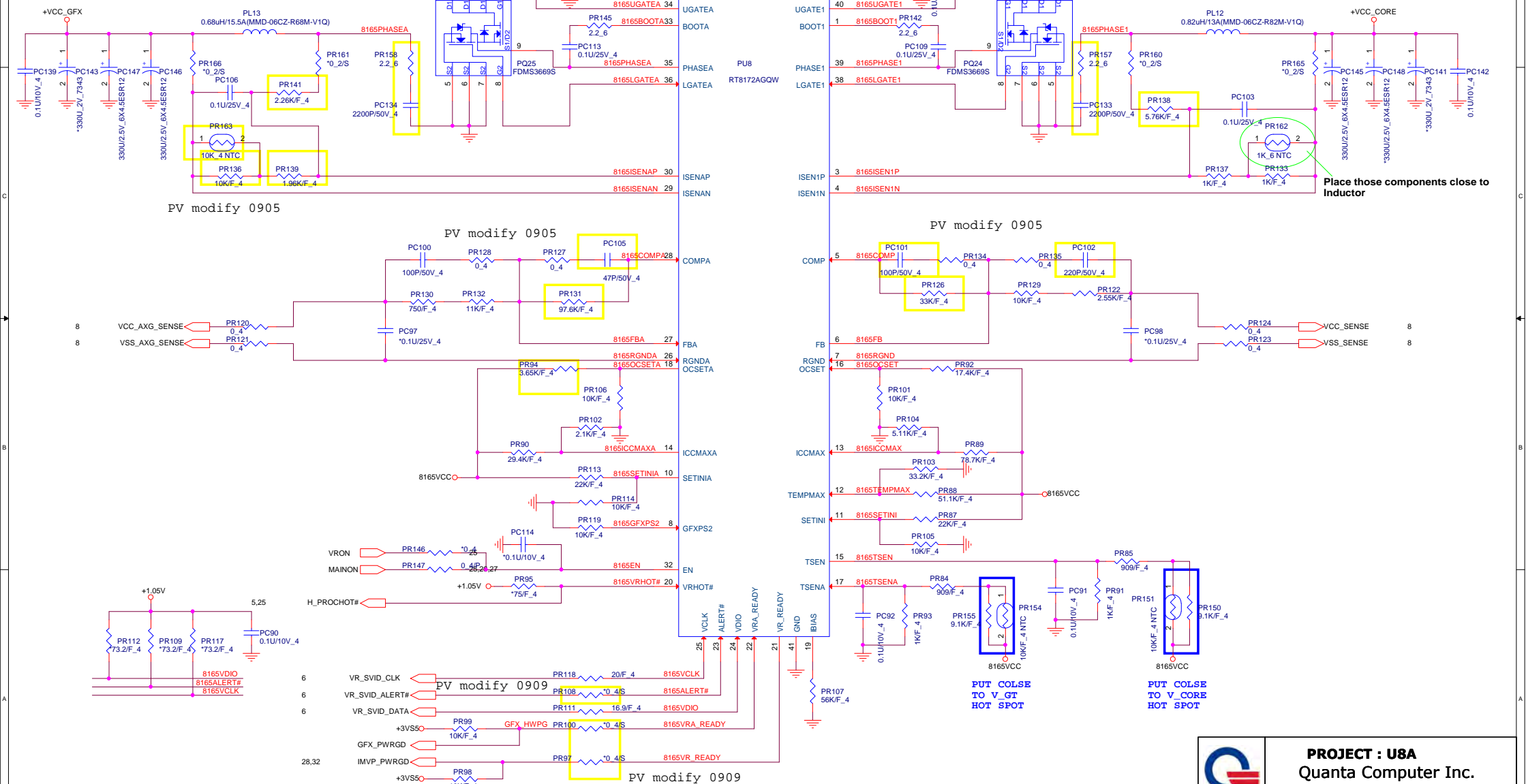


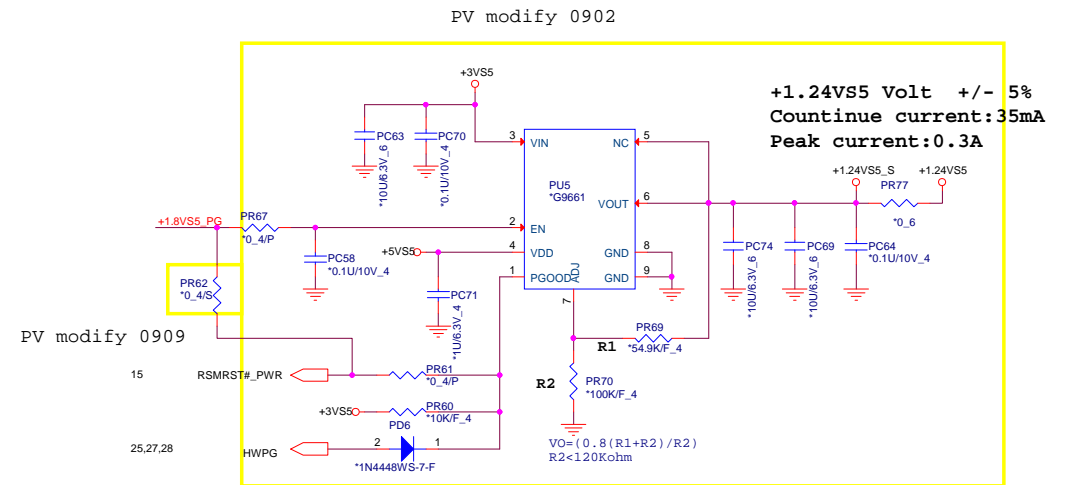
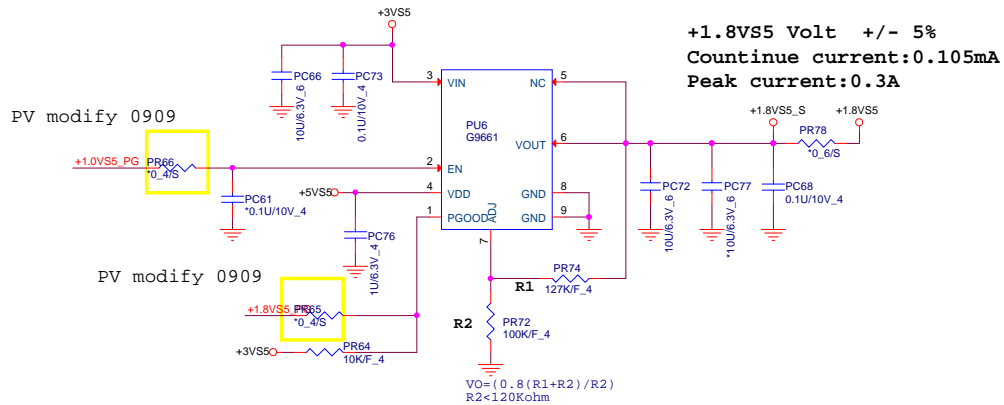
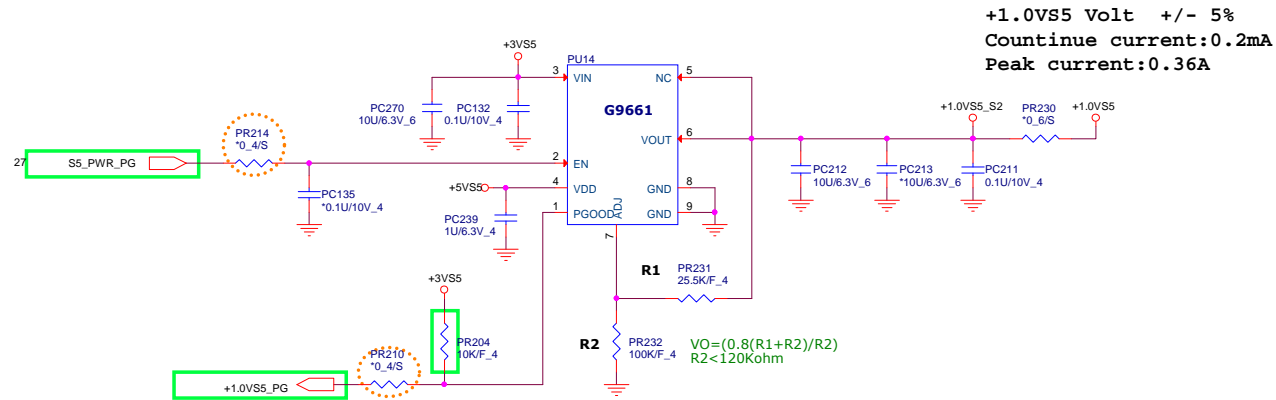
PROJECT : USA
Quanta Computer Inc.

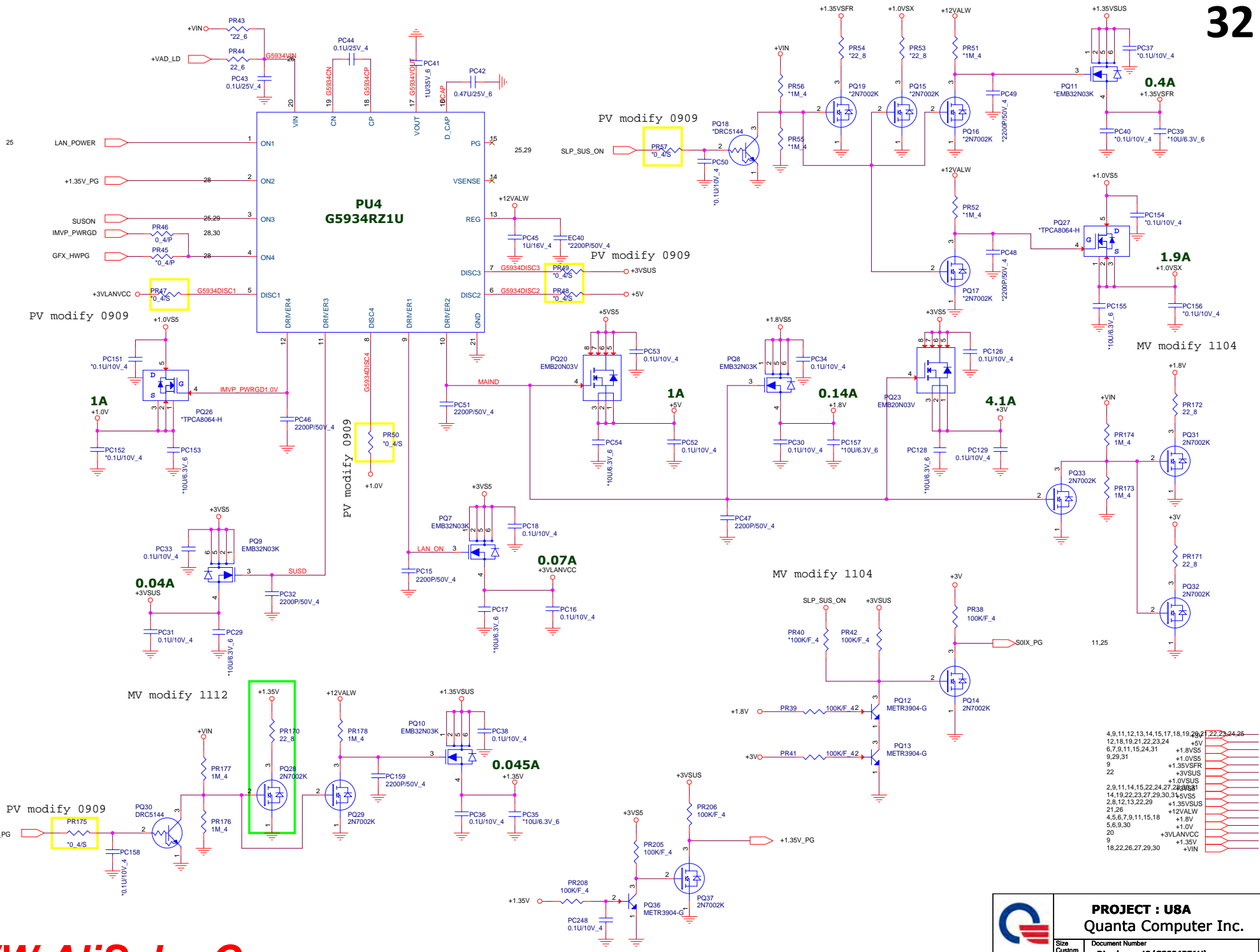
Size	Document Number	Rev
Custom	+1.05V/+1.5V (SY8002)	1A
Date: Thursday, April 23, 2015	Sheet 28 of 37	



+GFXORE Volt +/- 5%
Countinue current:6A
Peak current:14A
OCP minimum:16.5A







4,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25	+5V
12,18,19,21,22,23,24	+1.8VS5
6,7,9,11,15,24,31	+1.0VS5
9,29,31	+1.35VSFR
9	+3VSUS
22	+1.0VSUS
2,9,11,14,15,22,24,27,28,29,30,31	+1.35VSUS
14,19,22,23,27,29,30,31	+1.35VSUS
2,8,12,13,22,29	+1.35VSUS
21,26	+12VALW
4,5,6,7,9,11,15,18	+1.8V
5,6,9,30	+1.0V
20	+3VLAVCC
9	+1.35V
18,22,26,27,29,30	+VIN

USB3.0	Port Assignment	Power control pin
PORT0	USB HUB	

USB2.0	Port Assignment	Power control pin
PORT0	USB HUB	N/A
PORT1	Right side USB Daughter BD	USBPW_ON#(from EC)
PORT2	BT	N/A
PORT3	Camera	N/A

USB HUB	Port Assignment	Power control pin
USB30 PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
USB30 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB30 PORT3	N/A	
USB30 PORT4	N/A	
USB20 PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
USB20 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB20 PORT3	TS	TS_ON
USB20 PORT4		

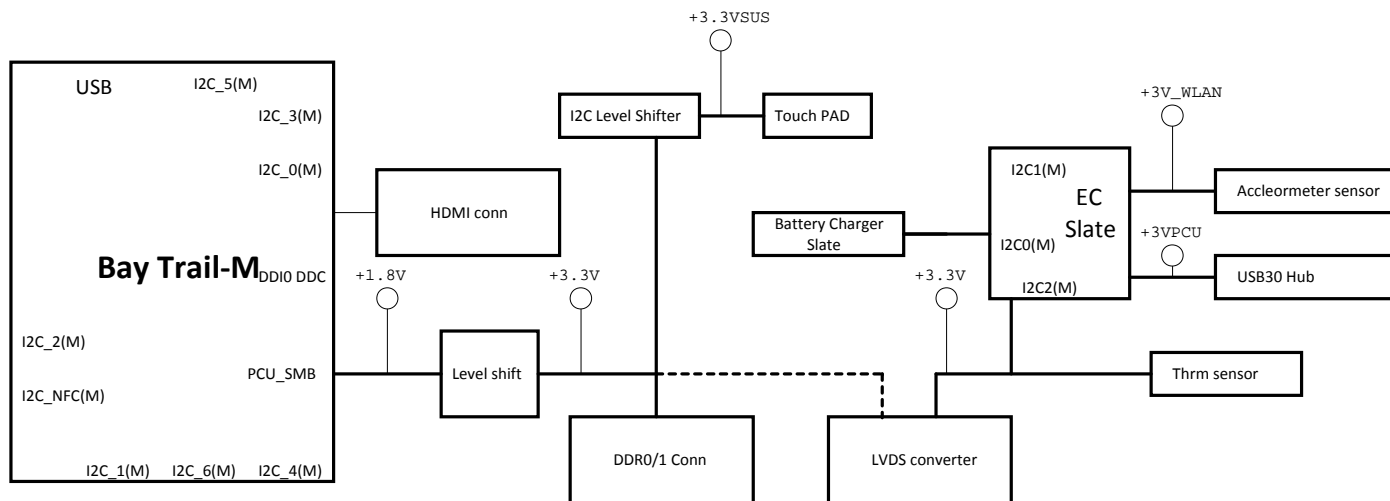
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	ODD	ZERO_PWR_ODD

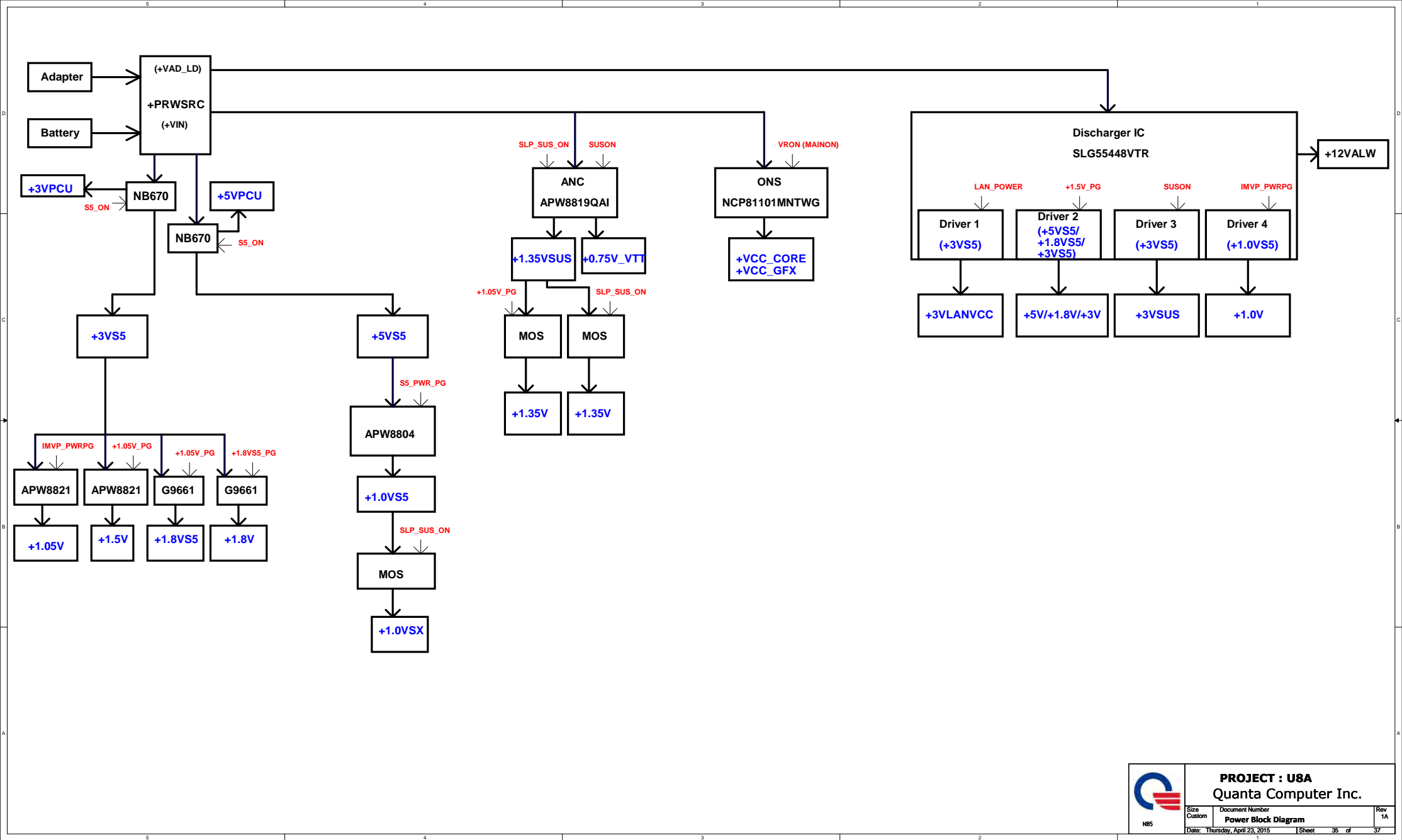
PCIE	Port Assignment	Control pin
PCIE 0	Card reader	
PCIE 1	WLAN	
PCIE 2	LAN	
PCIE 3	NC	

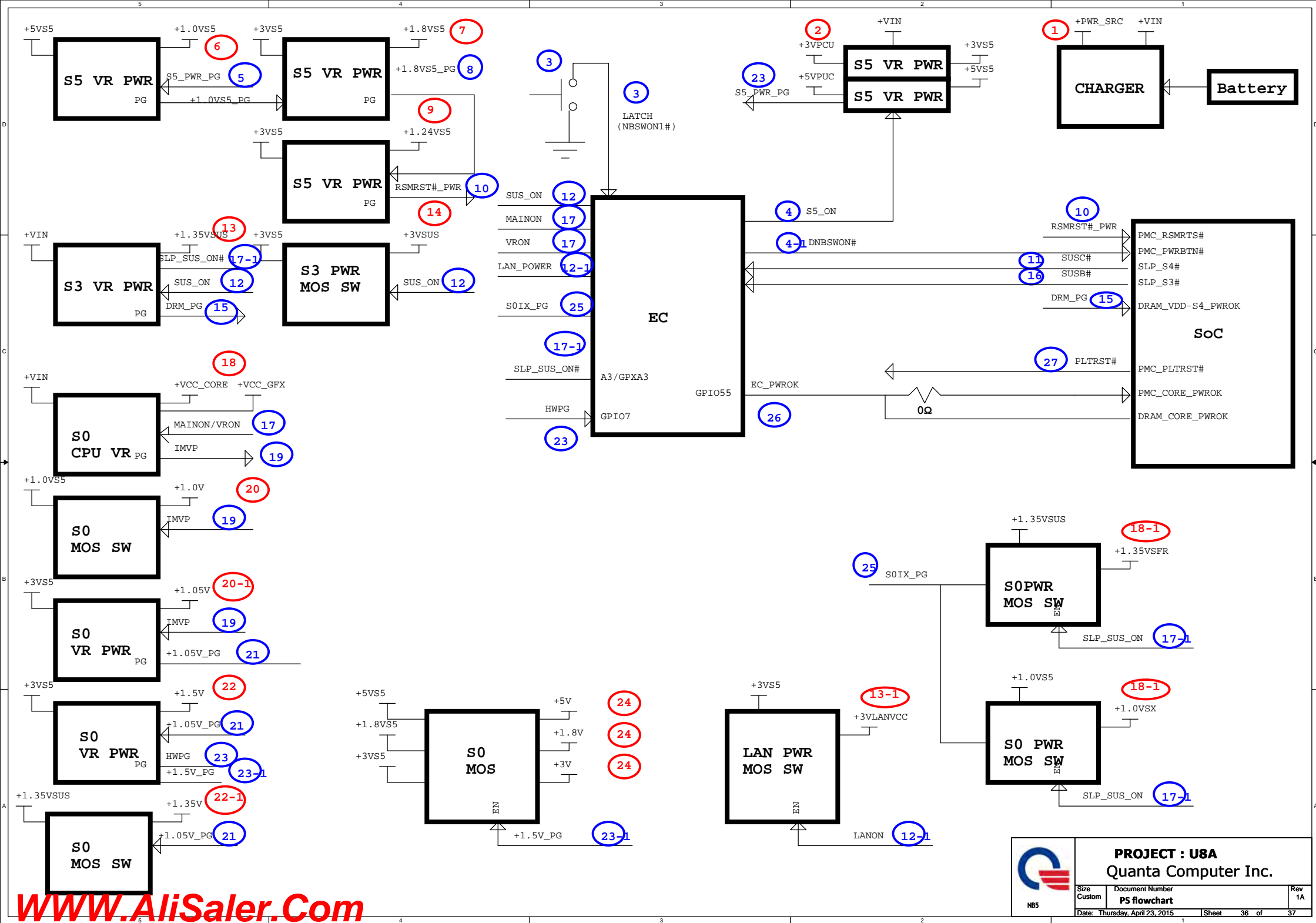


PROJECT : U8A
Quanta Computer Inc.

Size Custom	Document Number Data port assignment	Rev 1A
Date: Thursday, April 23, 2015	Sheet 33 of 37	

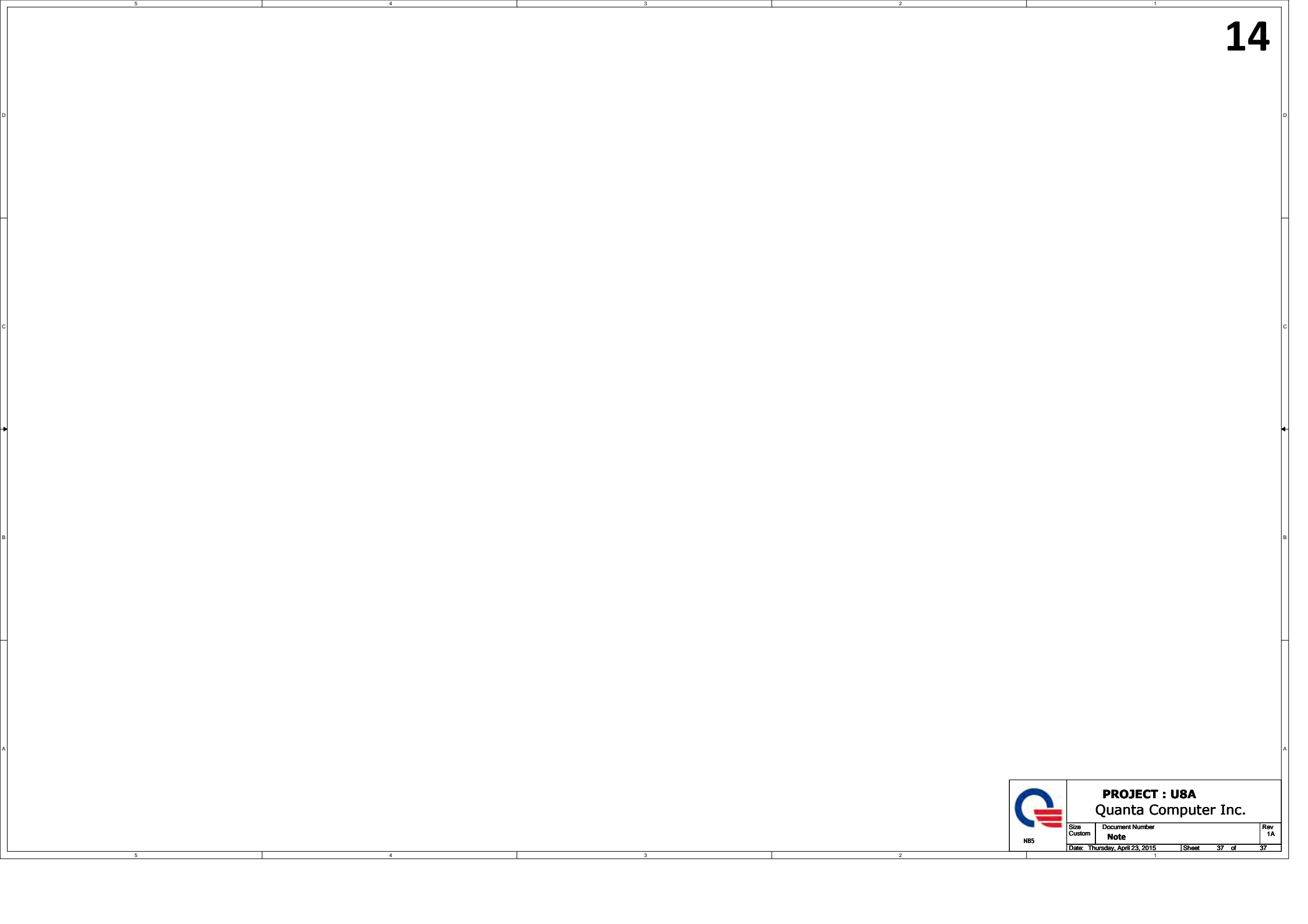







PROJECT : U8A
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Date: Thursday, April 23, 2015	PS flowchart	
Sheet 36 of 37		



 N85	PROJECT : USA Quanta Computer Inc.		
	Size Custom	Document Number Note	Rev 1A
	Date: Thursday, April 23, 2015		Sheet 37 of 37